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<u>L6</u>	l4 and L5	70	<u>L6</u>
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<u>L4</u>	l2 with l3	477	<u>L4</u>
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<u>L2</u>	cache near3(allocat\$ or manag\$ or setting)	10964	<u>L2</u>
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**1. A virtual cache-based workstation architecture**

Frink, C.R.; Roy, P.J.;  
Computer Workstations, 1988., Proceedings of the 2nd IEEE Conference on  
7-10 March 1988 Page(s):80 - 87

[AbstractPlus](#) | Full Text: [PDF](#)(568 KB) IEEE CNF



**2. The cache architecture of the Apollo DN4000**

Frink, C.R.; Roy, P.J.;  
Comcon Spring '88. Thirty-Third IEEE Computer Society International Conference, Digest of Pa  
29 Feb.-3 March 1988 Page(s):300 - 302

[AbstractPlus](#) | Full Text: [PDF](#)(240 KB) IEEE CNF



**3. A 2 K byte fully-associative cache memory with on-chip DRAM control**

Griffith, S.; Golson, S.;  
Custom Integrated Circuits Conference, 1989., Proceedings of the IEEE 1989  
15-18 May 1989 Page(s):10.2/1 - 10.2/5

[AbstractPlus](#) | Full Text: [PDF](#)(340 KB) IEEE CNF



**4. Proteus system architecture and organization**

Somani, A.K.; Wittenbrink, C.; Haralick, R.M.; Shapiro, L.G.; Jenq-Neng Hwang; Chung-Ho Cher  
Johnson, R.; Cooper, K.;  
Parallel Processing Symposium, 1991. Proceedings., Fifth International  
30 April-2 May 1991 Page(s):287 - 294

[AbstractPlus](#) | Full Text: [PDF](#)(764 KB) IEEE CNF



**5. Software-Controlled Cache Architecture for Energy Efficiency**

Yang, C.-L.; Tseng, H.-W.; Ho, C.-C.; Wu, J.-L.;  
Circuits and Systems for Video Technology, IEEE Transactions on  
Volume 15, Issue 5, May 2005 Page(s):634 - 644

[AbstractPlus](#) | Full Text: [PDF](#)(1040 KB) IEEE JNL



**6. Reducing contention in shared-memory multiprocessors**

Stenstrom, P.;  
Computer  
Volume 21, Issue 11, Nov. 1988 Page(s):26 - 37

[AbstractPlus](#) | Full Text: [PDF](#)(1104 KB) IEEE JNL



**7. QoS-adaptive proxy caching for multimedia streaming over the Internet**

Fang Yu; Qian Zhang; Wenwu Zhu; Ya-Qin Zhang;  
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- ☐ 8. **HotSpot Cache: Joint Temporal and Spatial Locality Exploitation for I-Cache Energy Redu.**  
Chia-Lin Chia-Lin Yang; Chien-Hao Lee;  
Low Power Electronics and Design, 2004. ISLPED '04. Proceedings of the 2004 International Symposium on  
2004 Page(s):114 - 119  
[AbstractPlus](#) | Full Text: [PDF\(208 KB\)](#) IEEE CNF
- ☐ 9. **Proteus: a reconfigurable computational network for computer vision**  
Haralick, R.M.; Somani, A.K.; Wittenbrink, C.; Johnson, R.; Cooper, K.; Shapiro, L.G.; Phillips, I.I  
Hwang, J.-N.; Cheung, W.; Yao, Y.H.; Chen, C.H.; Yang, L.; Daugherty, B.; Lorbeski, B.; Loving,  
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Proceedings., 11th IAPR International Conference on  
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- ☐ 10. **Modeling memory reference patterns of programs in cache memory systems**  
Mukkamala, R.; Agrawala, A.;  
Modeling, Analysis and Simulation of Computer and Telecommunication Systems, 1999. Procee  
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24-28 Oct. 1999 Page(s):288 - 295  
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- ☐ 11. **Compiler-directed resource management for active code regions**  
Sree, R.; Settle, A.; Bratt, I.; Connors, D.;  
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- ☐ 12. **HotSpot cache: joint temporal and spatial locality exploitation for I-cache energy reduction**  
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